10/065,822

1. (Currently Amended) An array of content addressable memory (CAM) cells, each of said CAM cells comprising:

a search line; and

a bitline parallel to said search line,

wherein across said array, search lines and bit lines of said CAM cells are interdigitated, such that said search lines and bitlines alternate across said array,

wherein said array includes macros comprising at least two of said CAM cells, and

wherein each of said macros includes a common match clock line shared by the CAM cells within each macro.

2. (Original) The array of CAM cells in claim 1, further comprising a top matchline and bottom matchline running perpendicular to said search line and said bitline.

3. (Currently Amended) The array of CAM cells in claim 1, wherein ~~said array includes macros comprising at least two of said CAM cells, and~~ within each of said macros one of the following structures exists:

a bit line is between two search lines; and

a search line is between two bit lines.

4. (Cancelled).

5. (Currently Amended) ~~The array of CAM cells in claim 3,~~ An array of content addressable memory (CAM) cells, each of said CAM cells comprising:

a search line; and

a bitline parallel to said search line,

wherein across said array, search lines and bit lines of said CAM cells are interdigitated, such that said search lines and bitlines alternate across said array,

wherein said array includes macros comprising at least two of said CAM cells, and

wherein layouts of adjacent macros are inverted with respect to one another.

6. (Currently Amended) ~~The array of CAM cells in claim 3,~~ An array of content addressable memory (CAM) cells, each of said CAM cells comprising:

a search line; and

a bitline parallel to said search line.

wherein across said array, search lines and bit lines of said CAM cells are interdigitated, such that said search lines and bitlines alternate across said array,

wherein said array includes macros comprising at least two of said CAM cells, and

wherein each of said macros comprise:

a top wordline; and

a bottom wordline;

wherein said top wordline and said bottom wordline cross between each of said CAM macros.

7. (Original) The array of CAM cells in claim 5, further comprising a match clock signal running through each of said macros, wherein said match clock signal includes a jog to accommodate said inverted layout of said adjacent macros.

8. (Original) A memory array comprising:

a plurality of content addressable memory (CAM) macros, wherein each of said macros includes at least two CAM cells,

wherein layouts of said macros are alternatively inverted with respect to one another within said array, such that layouts of each macro are inverted with respect to adjacent macros.

9. (Original) The memory array in claim 8, wherein each of said macros comprises:

a top wordline; and

a bottom wordline,

wherein, said top wordline and said bottom wordline cross between each of said macros.

10. (Original) The memory array in claim 8, further comprising a match clock signal running through each of said macros, wherein said match clock signal includes a jog to accommodate said inverted layout of said adjacent macros.

11. (Original) The memory array in claim 8, wherein each of said CAM cells comprises:

a search line; and

a bitline parallel to said search line,

wherein across said array, search lines and bit lines of said CAM cells are interdigitated, such that said search lines and bitlines alternate across said array.

12. (Original) The array of CAM cells in claim 11, further comprising a top matchline and bottom matchline running perpendicular to said search line and said bitline.

13. (Original) The array of CAM cells in claim 11, wherein within each of said macros one of the following structures exists:

a bit line is between two search lines; and

a search line is between two bit lines.

14. (Original) The array of CAM cells in claim 8, wherein each of said macros includes a common match clock line shared by the CAM cells within each macro.

15. (Original) A memory array comprising:

a plurality of content addressable memory (CAM) macros, wherein each of said macros includes at least two CAM cells,

wherein layouts of said macros are alternatively inverted with respect to one another

within said array, such that layouts of each macro are inverted with respect to adjacent macros and to balance parasitic capacitance across said array.

16. (Original) The memory array in claim 15, wherein each of said macros comprises:

a top wordline; and

a bottom wordline,

wherein, said top wordline and said bottom wordline cross between each of said macros.

17. (Original) The memory array in claim 15, further comprising a match clock signal running through each of said macros, wherein said match clock signal includes a jog to accommodate said inverted layout of said adjacent macros.

18. (Original) The memory array in claim 15, wherein each of said CAM cells comprises:

a search line; and

a bitline parallel to said search line,

wherein across said array, search lines and bit lines of said CAM cells are interdigitated, such that said search lines and bitlines alternate across said array.

19. (Original) The array of CAM cells in claim 18, further comprising a top matchline and bottom matchline running perpendicular to said search line and said bitline.

20. (Original) The array of CAM cells in claim 18, wherein within each of said macros one of the following structures exists:

a bit line is between two search lines; and

a search line is between two bit lines.